TASK QUARTERLY 2 No 1 (1998), 73-83

COMPUTER ANALYSIS OF THE CURRENT–REGULATED DELTA MODULATOR WITH HEXAGONAL QUANTIZER

JANUSZ NIEZNAŃSKI AND KRZYSZTOF IWAN

Department of Electrical and Control Engineering
Technical University of Gdansk
Narutowicza 11, 80-952 Gdansk, Poland

Abstract: This paper reports extensive simulation research into the use of the hexagonal quantizer in current-regulated delta modulators (CRDMs) for ac motor drive applications. It is demonstrated that the hexagonal quantizer with an appropriately selected threshold significantly lowers the current harmonic distortion and dramatically reduces the switching frequency of inverter devices, as compared to the conventional CRDM. Basic information is given on how the simulations were organized and sequenced to ensure fast steady-state convergence, as well as minimize the required data transfers.

1. Introduction

A steady interest can be observed within the power electronics community in the issue of current control; the reason for this is the vital role of current control in high-performance ac motor drives. For a review and a comprehensive list of references on current control techniques, see [1]. From the viewpoint of the timing structure, current controllers can be divided into the following three categories:

a) PWM current controllers,

b) PDM current controllers,

c) hysteresis (or tolerance-band) current controllers.

The controllers belonging to categories (a) and (b) rely on externally generated regular timing patterns, while the hysteresis controllers exhibit irregular, limit-cycle type of timing. The concern here is with the PDM (pulse density modulation) based current controllers. Such controllers are timed by constant-frequency clock sequences; the inverter output vectors are only updated at clock instants and remain unaltered within a clock period (that is, there is no duty cycle control of output pulses). This kind of modulation is not as effective as the PWM in shaping the spectral quality of the

output waveforms, but has two important advantages: (*i*) it requires only a single timer, which is particularly attractive in microprocessor or DSP implementations; (*ii*) it can be used to control inverter topologies that do not allow PWM (e.g. the popular resonant dc link inverter [2, 3]). Furthermore, current-controlled PDM can be based on infinite-gain error amplifiers (comparators), and thereby exhibit excellent dynamic response, similar to that of hysteresis controllers [3] (while, at the same time, the switching frequency remains well under control).

By far the most popular PDM current controller is the *current-regulated delta modulator*, CRDM (e.g. [2, 3]). Conventional CRDMs, Figure 1, use three independent sampling comparators, one for each phase. The high level at a comparator output

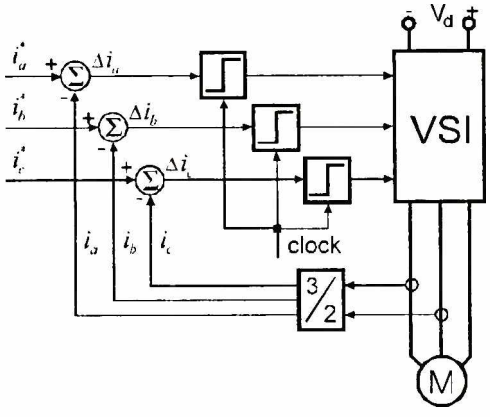

Figure 1. *Block diagram of the conventional current-regulated delta modulator (VSI = voltage source inverter)*

turns on the upper switch in its corresponding inverter leg, while the low level turns on the lower switch. The resultant inverter output vs. current error transfer characteristic is depicted in Figure 2. The dashed lines delineate the current error positions and

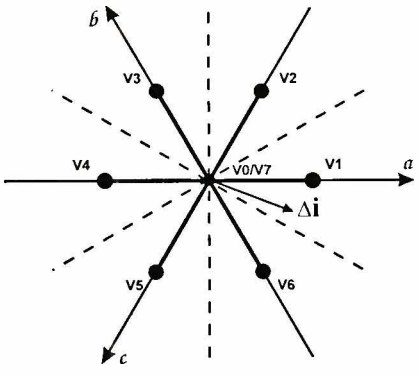

Figure 2. *Principle of selecting inverter output vectors in the current-regulated delta modulator of Figure 1*

their corresponding inverter output vectors. The zero vectors (V0 and V7) are selected with probability zero, meaning that they are not used by this arrangement. The use of a three-phase clock has been suggested [4] as a method whereby the zero vectors can be made accessible. This technique improves the spectral quality of the generated currents, but the effective switching rate of the inverter devices remains essentially unchanged [4]. Clearly, the applicability of this technique is confined to hard-switched inverters.

The objective of this work is to examine a generalized CRDM, as derived from the sigma-delta modulator (SDM) with *hexagonal quantizer*. The latter modulator was first suggested in [5], while in [6] it was derived as a solution of an optimization problem. The following section shortly introduces the above modulator and shows the passage to the equivalent delta modulator.

2. Hexagonal quantization in sigma-delta and delta modulators

The block diagram of the SDM with hexagonal quantizer is shown in Figure 3,

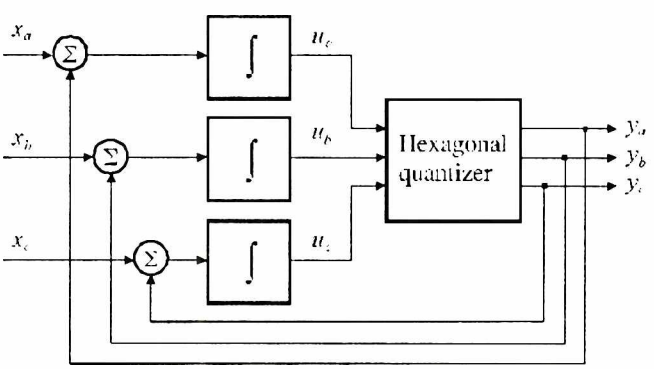

Figure 3. *Sigma-delta modulator with hexagonal quantizer*

while Figure 4 presents the characteristic and a block diagram of the quantizer itself. If the normalized quantizer threshold is 0.5, then an SDM with this quantizer produces the minimum-distortion output waveforms, the minimization criterion being the power or rms error between the integrated input and integrated output of the modulator (the integration can be considered to mimic the filtering action of the load inductance). Strictly speaking, the waveforms produced by such a modulator are exact replicas of the minimum-distortion waveforms delayed by one clock period (for details, see [6]). Now, by shifting the integrators in Figure 3 in front of the summing junctions, an equivalent scheme is obtained (Figure 5), which can be viewed as a connection of an integrator and a delta modulator. Interpreting the output of the first integrator as the commanded current, and the output of the feedback integrator as the actual (controlled) current, it is clear that this current control arrangement inherits the distortion-minimization property of the original SDM. Finally, by replacing the

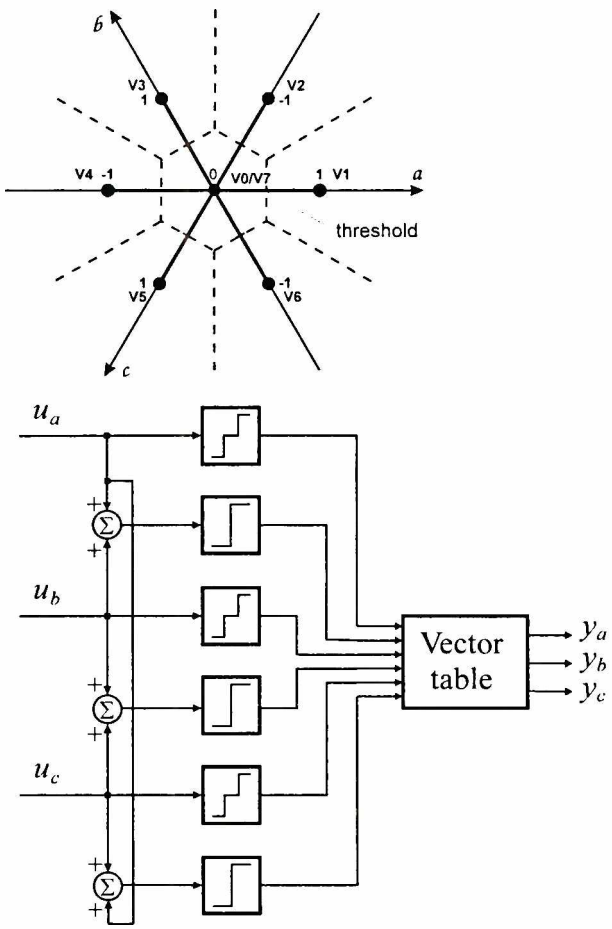

Figure 4. *Normalized characteristic of hexagonal quantizer and the corresponding block diagram*

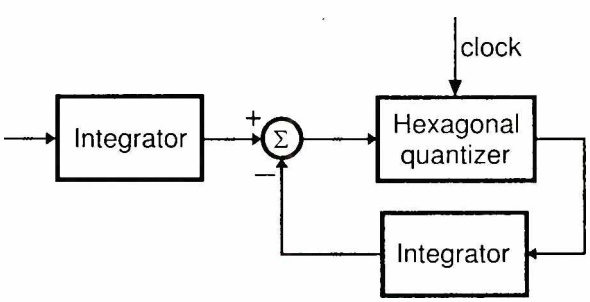

Figure 5. *Sigma-delta modulator represented as a connection of an integrator and a delta modulator*

quantizer in Figure 5 with an equivalent connection of inverter vector selector and the inverter itself, and substituting an inductor for the integrator, one arrives at the CRDM. Because the optimum threshold value of 0.5 for the quantizer was established assuming a unity clock period, a unity magnitude of the output voltage vectors, and a unity

integrator gain, it is convenient to rescale this threshold so that it reflects the actual values of the above quantities. By reinspecting the developments contained in [6] it can be concluded that the normalized threshold value equals its absolute value divided by the magnitude of the integral, over one clock period, of the output vector. Thus, the denormalized expression for the optimum threshold is

$$\text{optimum threshold} = 0.5\alpha\, bT_{\text{CLK}} \tag{1}$$

where α is the integrator gain, T_{CLK} is the clock period, and b is the average magnitude of the quantizer output vector. For a hard-switched VSI, substituting $\alpha = 1/L$ and $b = 2/3V_{\text{d}}$, one obtains :

$$I_{\text{th}} = \frac{1}{3} \cdot \frac{V_{\text{d}} \cdot T_{\text{CLK}}}{L} \tag{2}$$

with V_{d} being the dc link voltage, while L represents the load inductance.

By way of digression, the so derived current controller shows major resemblance to the one reported in [2] (dubbed *adjacent-state current regulator*, ASCR), in that the latter also relies on a hexagonal error region for the zero vector selection. The ASCR, however, has somewhat cumbersome structure, is more nested in time (previously selected vector is involved in the new vector selection), and requires explicit evaluation of the magnitude of the current error. Moreover, no guidance is given in the above report on the selection of the width of the hexagon.

A three-phase CRDM with hexagonal quantizer was simulated in MATLAB using a simple discrete-time model, similar to that considered in [6]. To confirm the theoretically predicted distortion-minimization property of this controller, the quantizer threshold was assigned a number of different values in each simulation; these values were of the form $h \cdot I_{\text{th}}$, $h = 0, 0.1, \ldots, 1.5$. An example set of results is given in Figure 6. The parameters used in the simulations were the following: modulation index

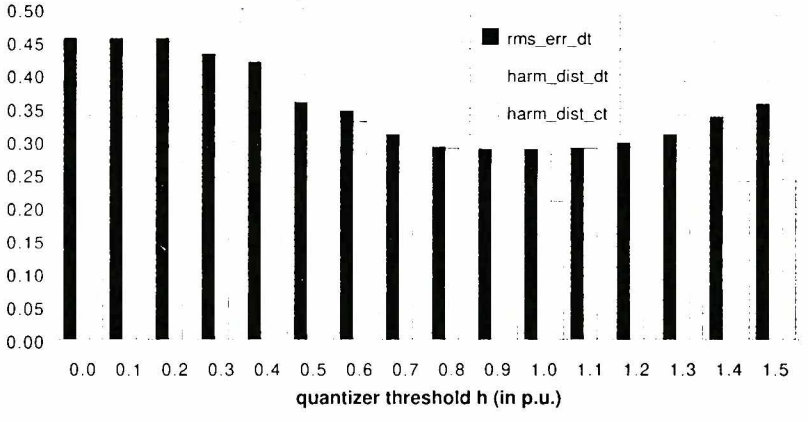

Figure 6. *Example simulation results of current-regulated delta modulator with hexagonal quantizer (inductive load)*

$m_a = 0.75$, frequency modulation ratio $m_f = 252$, $T_{CLK} = 80\mu s$, $L = 4.64mH$, $V_d = 100V$. Note that if $h = 0$, the quantizer characteristic reduces to that of the conventional CRDM shown in Figure 2, meaning that the latter controller was also included in the simulations. Figure 6 contains three different distortion characteristics. The "rms_err_dt" characteristic represents the discrete-time rms current error evaluated with the assumed one clock period delay between the reference current and the actual current (**i***[k-1] - **i**[k]). The "harm_dist_dt" characteristic is a discrete-time harmonic distortion current, while the "harm_dist_ct" is a continuous-time harmonic distortion current (because the discrete-time model analyzed in MATLAB does not explicitly produce continuous-time current waveforms, the latter characteristic was computed using the principle of factoring PAM signal spectra [7]). The "rms_err_dt" quantity is exactly the quantity for which the theoretical minimum has been located in [6], while of the ultimate interest is the minimum of the "harm_dist_ct" characteristic. As seen in Figure 6, the three characteristics considered have similar shape, and the minima all occur at the theoretically predicted threshold value of $h = 1$. This confirms the underlying theory and demonstrates that the discrete-time rms current error is a valid quality measure for synthesizing optimum PDM controllers. However, for comparative studies it is convenient to separate the harmonic and linear distortion, and thus to rely on frequency-domain analysis (this is particularly true for motor loads, where the counter EMF causes significant linear distortion).

Thus far it has been confirmed that the CRDM with hexagonal quantizer and $h = 1$ is a minimum-distortion PDM current controller if the load is purely inductive. By way of digression, note that considerable interest is also located in voltage-control applications of the delta modulation principle [8, 9]. The most pronounced feature of such controllers, having an integrating local feedback and using sampling [8] or hysteresis [9] comparators, is that they possess an inherent V/f = const characteristic. For the sampling (i.e. PDM-type) variety of such controllers it will again be the hexagonal quantizer with a threshold determined from (1) that will minimize the distortion of the current through an inductive load supplied from this type of controller.

In addition to minimizing the waveform distortion, the use of hexagonal quantizer leads to active selection of zero vectors, whereby the effective device switching frequency can significantly be reduced. This aspect was given particular attention while simulating the CRDM with an induction motor load (see the following section).

3. Motor current control via CRDM with hexagonal quantizer

Extensive simulation analyses have been carried out for the CRDM with a squirrel-cage induction motor load. Since the whole simulation schedule included hundreds of computationally intensive steady-state analyses, it called for special tools and techniques. The simulations were performed using the Unix version of the TCad simulator, developed at the Technical University of Gdansk. To speed up steady-state convergence, the following simple methodology was adopted: first, the motor startup

was analyzed in a slip-control drive configuration using current controlled current sources, Figure 7; then, the state variables pertaining to the motor and the controller

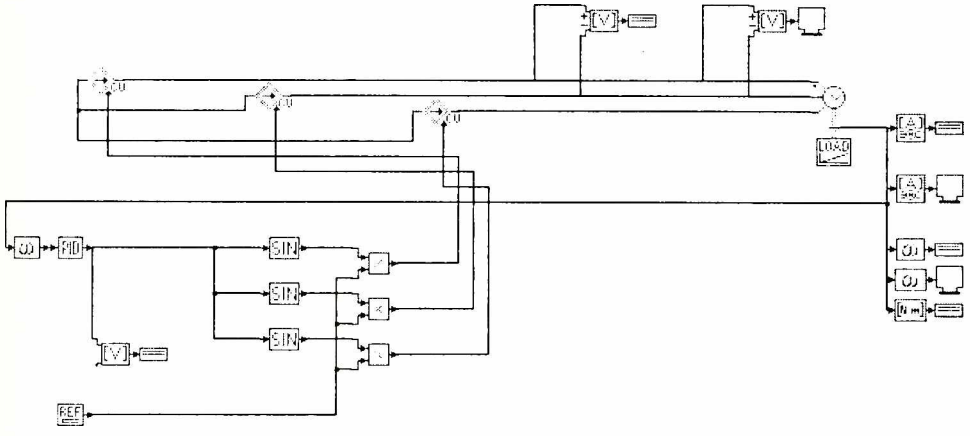

Figure 7. *Schematic task definition for fast estimation of the steady state*

under steady state were used as the initial condition for a simulation in the same control arrangement with the CRDM replacing the controlled sources, Figure 8; this

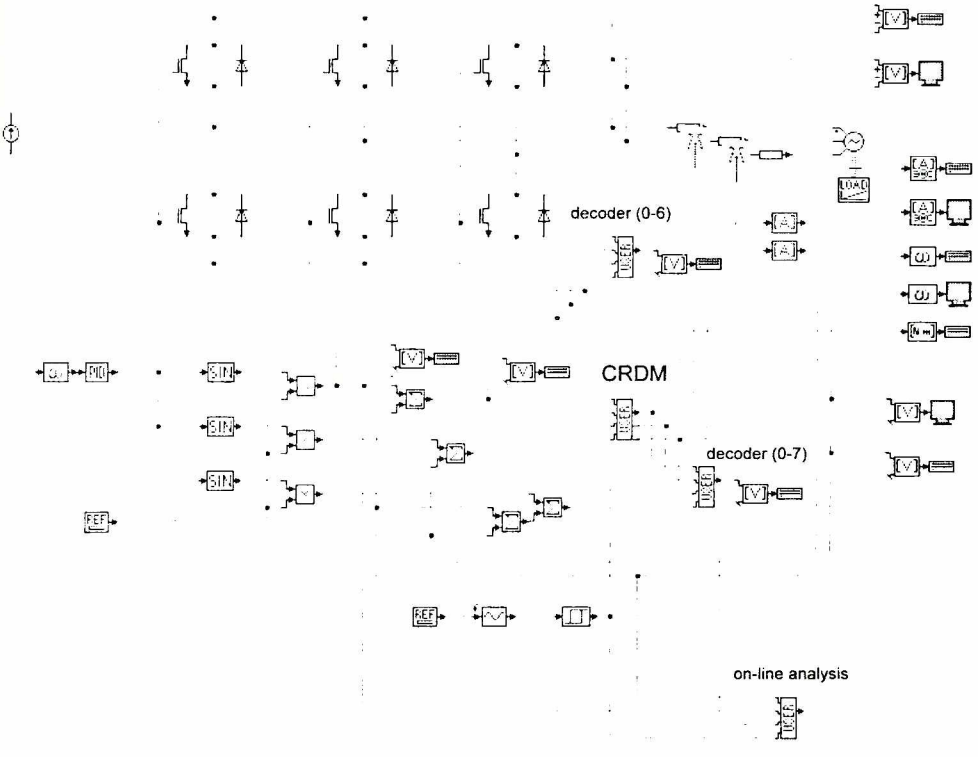

Figure 8. *Schematic task definition for the analysis of the induction motor loaded current-regulated delta modulator*

second simulation was aimed at finding a more precise estimation of the steady state values; and finally, the latter values were used as the initial condition in a series of 16 simulation runs, each with a different value of the quantizer threshold h. The above technique was repeated for each of the motor steady state speeds included in the analyses. To avoid time consuming waveform data transfers between the remote Unix computer and the local PC, and eliminate the subsequent manually controlled postprocessing, the waveform analyses were performed during the simulation runs by means of an appropriately programmed user-defined unit (labeled "on-line analysis" in Figure 8). The final simulation runs took ca. 15 seconds each (for motor speeds close to the synchronous speed), meaning about 4 minutes per a full series of 16 runs. Some of the results obtained are collected in Figs. 9 and 10. Concerning the harmonic

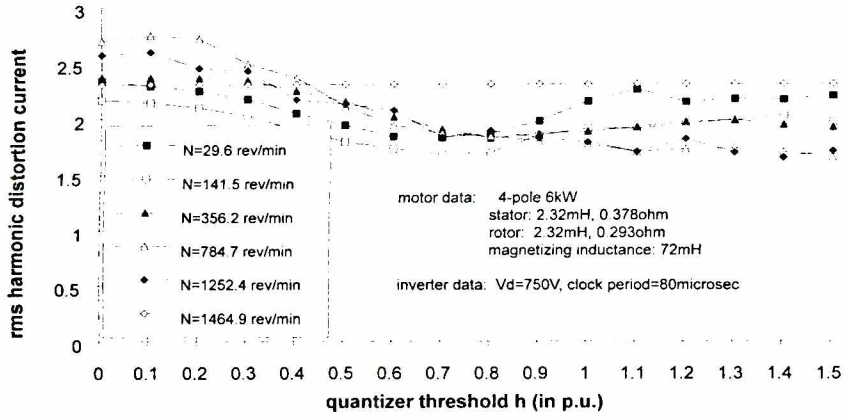

Figure 9. *Simulated harmonic distortion vs. hexagonal quantizer threshold for current-regulated delta modulator with squirrel-cage induction motor load*

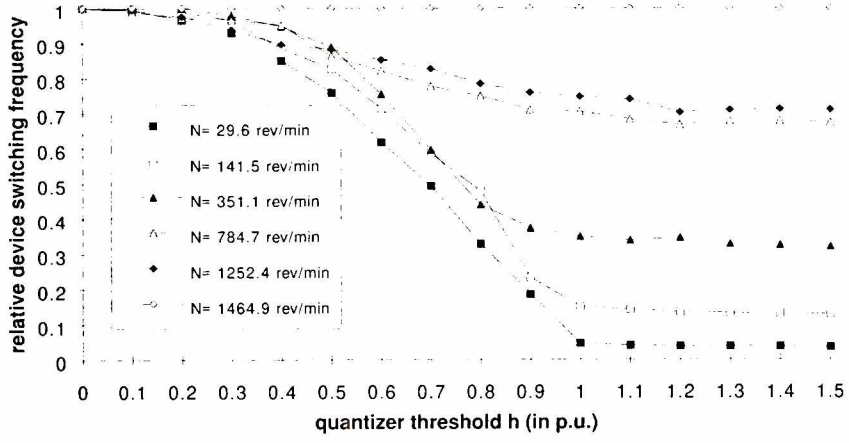

Figure 10. *Simulated inverter device switching frequency vs. hexagonal quantizer threshold for current-regulated delta modulator with squirrel-cage induction motor load*

distortion (Figure 9), it is seen that the minimum location wanders above and below $h = 1$ as the motor speed varies, but the distortion at $h = 1$ is considerably lower than that at $h = 0$ (conventional CRDM). For instance, the squared ratio of the distortion (i.e. the power ratio) at $h = 0$ to that at $h = 1$ for a medium motor speed (748.7 rev/min) is as high as 2.32. This ratio decreases at both lower and higher speeds.

The most pronounced differences between characteristics obtained for different quantizer thresholds are seen in the relative device switching frequency (Figure 10). A dramatic reduction in this quantity occurs at low speed for the threshold values $h = 1$ or higher. To illustrate this phenomenon, Figure 11 shows the current waveforms

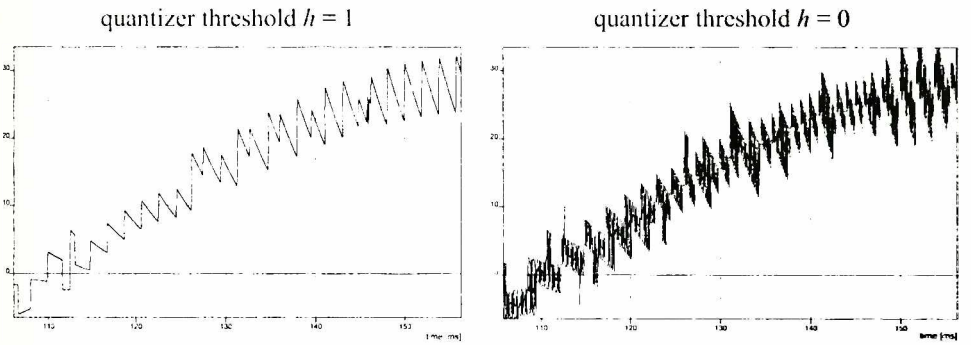

Figure 11. *Current waveforms (quarter period) corresponding to the motor speed of 29.6 rev/min*

corresponding to the motor speed of 29.6 rev/min for $h = 1$ and $h = 0$. At higher speeds the improvement in the switching frequency is not as tremendous, but still significant. This effect stems from the fact that for $h = 1$ (and higher) the CRDM systematically applies the zero vectors, never selected for $h = 0$ (Figure 12). Because of this, the line-line inverter voltages are free, or almost free, from what is called ±1 transitions, a favorable feature in itself.

Aside from the above advantages of the CRDM with hexagonal quantizer and $h = 1$, a serious drawback has also been observed which affects the CRDM in general; namely, this controller fails to accurately reconstruct the commanded amplitude at high speeds (i.e. when the counter EMF has large amplitude and the phase angle between the counter EMF and the reference current is small). This is not merely a problem of a decrease in the available current slewing voltage. There is a mention on the above effect in [3], where it is attributed to "the migration of the current ripple boundary" [3]. The problem is now under study.

4. Conclusion

The use of the hexagonal quantizer in current-regulated delta modulators has been suggested, based on earlier work pertaining to the sigma-delta modulation. Extensive simulation analyses have been reported which confirm the theoretical prediction that the CRDM with an inductive load produces minimum current distortion when the

relative quantizer threshold is set to $h = 1$. When the CRDM operates with a motor load, the optimum setting for the threshold varies with the motor speed, but $h = 1$ remains to be significantly better than $h = 0$ (the latter setting representing the conventional CRDM). The most striking advantage of using the hexagonal quantizer with $h = 1$ is the tremendous reduction in the effective device switching frequency, particularly at lower speeds. A serious problem that has been observed, and calls for an effective cure, is the large amplitude errors occurring at higher speeds.

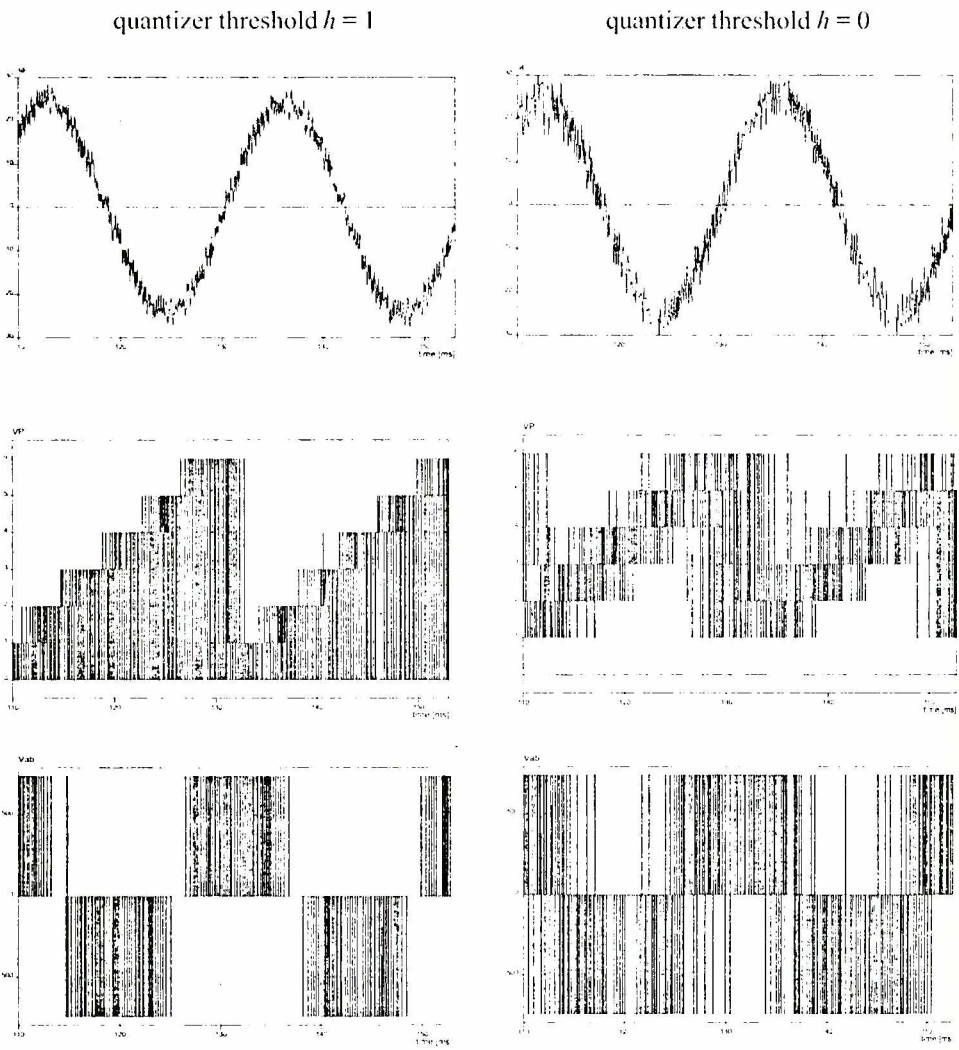

Figure 12. *Motor current, inverter output vector, and line-line voltage waveforms corresponding to the motor speed of 1252.4 rev/min*

Acknowledgments

The simulations presented throughout this report were performed on computers managed by the Academic Computer Centre in Gdansk (TASK).

References:

[1] Kaźmierkowski M. P., Dzieniakowski M. A., *Review of current-regulation techniques for three-phase PWM inverters*, IECON'94, **1**, (1994), pp. 567-575

[2] Habetler T. G., Divan D. M., *Performance characterization of a new discrete pulse-modulated current regulator*, IEEE Trans. Ind. Appl., **IA-25**, (1989), pp. 1139-1148

[3] Lorenz R. D., Divan D. M., *Dynamic analysis and experimental evaluation of delta modulators for field-oriented ac machine current regulators*, IEEE Trans. Ind. Appl., **IA-26**, (1990), pp. 296-301

[4] Dzieniakowski M. A., Kaźmierkowski M. P., *Microprocessor-based novel current regulator for VSI-PWM inverters*, PESC'92, **1**, pp. 459-464

[5] Luckjiff G., Dobson I., Divan D. M., *Interpolative sigma delta modulators for high frequency power electronic applications*, PESC'95, **1**, pp. 444-449

[6] Nieznański J., *Minimum-distortion pulse density modulation*, EDPE'96, **1**, pp. 94-99

[7] Gray R. M., Goodman J. W., *Fourier Transforms. An Introduction for Engineers*, Kluwer Academic Publishers, Boston 1995

[8] Karybakas C. A., *A DC to AC inverter based on the delta modulation principle*, Int. J. Electron., **49**, (1980), pp. 59-66

[9] Joos G., Ziogas P. D., *On maximizing gain and minimizing frequency of delta modulated inverters*, IEEE Trans. Ind. Electron., **IE-40**, (1993), pp. 436-444